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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/867,375	BERTSCH ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-29* is/are allowed.

6)☒ Claim(s) *1-7,9-17, and 30-36* is/are rejected.

7)☒ Claim(s) *8 and 18-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-36 of U.S. Application 09/867,375 filed on 10/4/2004 are presented for examination.

Claim Interpretation

2. Examiner interprets the claimed "Geometric Parameters" correspond to the parameters listed in the table next to paragraph 22 of the specification: "Effective Transistor Channel Length", "Gate Oxide Thickness", "Change in Device Width."
3. Examiner interprets the claimed "DC Parameters" correspond to the parameters listed in the table next to paragraph 22 of the specification: "Saturated Source / Drain Current", "Saturation Threshold Voltage", and "Linear Threshold Voltage".
4. Examiner interprets the claimed "AC Parameters" correspond to the parameters listed in the table next to paragraph 22 of the specification: "Overlap Capacitance", "Source/Drain Junction Capacitance", and "Sheet Resistance."
5. Examiner interprets the claimed "Delay Parameters" as corresponding to the parameter listed in the table next to paragraph 22 of the specification: "Delay per stage of Kerf Performance Screen Ring Oscillator."

Allowable Subject Matter

6. Claims 24-29 are allowed.

7. In regards to Independent Claim 24,

24. A method of performing model to hardware correlation for semiconductor chips, comprising:
obtaining fabrication in-line parametric data;
extracting first parameters from said parametric data to make a first set of go-data;
calculating a first simulated threshold voltage saturation and first simulated saturated source/drain current based on said first set of go-data using a modeling program;
performing a first comparing of said first simulated threshold voltage saturation to an in-line parametric threshold voltage saturation from said parametric data and a first comparing of said first simulated saturated source/drain current to an in-line parametric saturated source/drain current from said parametric data;
calculating a threshold voltage adder from said first comparing;
adding said threshold voltage adder to said first set of go-data to make a second set of go-data;
calculating a second simulated threshold voltage saturation and second simulated saturated source/drain current based on said second set of go-data using said modeling program;
performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current;
calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data;
calculating a simulated delay-per-stage based on said third set of go-data using said modeling program;
performing a third comparing of said simulated delay-per-stage to an in-line parametric delay-per-stage from said parametric data;
calculating a delay-per-stage error based on said third comparing process;
adding said delay-per-stage error to said third set of go-data to make a final set of go-data; and
correcting said modeling program using said final set of go-data.

The Strojwas reference teaches obtaining fabrication data and extracting parameters from this data (see Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6).

The Michaels reference expressly teaches comparing simulated threshold voltage saturation to the extracted data of threshold voltage saturation and

comparing simulated saturated source/drain current to the extracted data of saturated source/drain current. (See Sections 2 and 3.1).

The Bryant reference expressly teaches the monitoring and testing of hysteresis (delay) effects for control of a wafer manufacturing process (See Bryant, col.1, "Summary of the Invention"). Bryant also expressly teaches the importance of knowing the number of stages for estimating the delay. (see Bryant, col.2, lines 49-55).

However, neither Strojwas, nor Michael, nor Bryant expressly teach the following limitation:

- Removing defective chips from the first parameters to make a first set of go-data;

Moreover, the three references do not expressly teach, either individually or in combination, the specific combination of steps recited in the claim pertaining to performing the specific "first comparing" step, a "second comparing" step, a "third comparing" step, and final "correcting steps" that are described in detail in the claim.

8. Claims 25-28 depend from Claim 24, and therefore are also allowed for the same reasons as for Claim 24.

9. In regards to Independent Claim 29, Strojwas teaches the following limitations:

29. A method of performing model to hardware correlation for semiconductor chips, comprising:
obtaining fabrication line parametric data;
extracting first parameters from said parametric data;
removing defective chips from said first parameters to make a first set of go-data;
calculating a first simulated threshold voltage saturation and first simulated saturated source/drain current based on said first set of go-data using a modeling program;

performing a first comparing of said first simulated threshold voltage saturation to an in-line parametric threshold voltage saturation from said parametric dam and a first comparing of said first simulated saturated source/drain current to an in-line parametric saturated source/drain current from said parametric data;

calculating a threshold voltage adder from said first comparing;

adding said threshold voltage adder to said first set of go-data to make a second set of go-data;

calculating a second simulated threshold voltage saturation and second simulated saturated source/drain current based on said second set of go-data using said modeling program;

performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current;

verifying that said threshold voltage adder corrected said second simulated threshold voltage saturation and said second simulated saturated source/drain current;

calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data;

calculating a simulated delay-per-stage based on said third set of go-data using said modeling program;

performing a third comparing of said simulated delay-per-stage to an in-line parametric delay-per-stage from said parametric data;

calculating a delay-per-stage error based on said third comparing process;

adding said delay-per-stage error to said third set of go-data to make a final set of go-data;

outputting statistics based on said threshold voltage adder, said percentage error and said delay-per-stage error;

performing a fourth comparing of parametric yield data from said final set of go-data to functional yield data from wafer final test servers;

selecting acceptable chips which have good parametric yield data and good functional yield data from said fourth comparing process;

creating a model to hardware wafer map showing locations of said acceptable chips; and

performing a model to hardware comparison using said model to hardware wafer map.

The Strojwas reference teaches obtaining fabrication data and extracting parameters from this data (see Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6).

The Michaels reference expressly teaches comparing simulated threshold voltage saturation to the extracted data of threshold voltage saturation and comparing simulated saturated source/drain current to the extracted data of saturated source/drain current. (See Sections 2 and 3.1).

The Bryant reference expressly teaches the monitoring and testing of hysteresis (delay) effects for control of a wafer manufacturing process (See Bryant, col.1, "Summary of the Invention"). Bryant also expressly teaches the importance of knowing the number of stages for estimating the delay. (see Bryant, col.2, lines 49-55).

However, neither Strojwas, nor Michael, nor Bryant expressly teach the following limitation:

- Removing defective chips from the first parameters to make a first set of go-data;

Moreover, the three references do not expressly teach, either individually or in combination, the specific combination of steps recited in the claim pertaining to performing the specific "first comparing" step, a "second comparing" step, a "third comparing" step, and final "correcting steps" that are described in detail in the claim.

Claim Objections

10. Claims 8 and 18-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
11. In regards to Claims 8 and 23, neither Strojwas, Michaels, or Bryant, individually or in combination, expressly teach the removing of defective devices from the test parametric data, as recited in the following limitations:

8. The method in claim 1, further comprising identifying defective devices and removing said defective devices from said in-line test parametric data.

23. The method in claim 16, further comprising, after said extracting, removing defective chips from said first parameters to make said first set of go-data.

12. In regards to Claim 18, neither Strojwas, Michaels, or Bryant, individually or in combination, expressly teach the following limitation:

18. The method in claim 17, further comprising calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data.

13. Claims 19-22 all depend from Claim 18, and therefore are also objected to for the same reasons as Claim 18.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. The prior art used for these rejections is as follows:

16. Strojwas, A.J., "Design for Manufacturability and Yield". Proc. of the 26th ACM/IEEE Conf. on Design Automation. 1989. pp.454-459. (Henceforth referred to as "**Strojwas**").

17. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

18. **Claims 1, 9, 12-13, 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Strojwas.**

19. In regards to Claim 1, Strojwas teaches the following limitations:

1. A method of performing model to hardware correlation, comprising:

simulating models based upon design criteria;
(Strojwas, especially: Figure 3, "Performance Distributions", and associated text in Sections 4 and 5; Figure 4, "Design Rules", and associated text in Section 6)

manufacturing devices based upon said design criteria;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that one must manufacture devices in order to obtain "data fabrication lines" and to "defect statistics".

evaluating features of said devices during said manufacturing to produce in-line test parametric data;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that one must measure ("evaluate") features in order to obtain data and statistics.

comparing said models to said in-line test parametric data to obtain correlation data; and
(Strojwas, especially: Figure 3, "Do They Match?" and associated text in Sections 4 and 5; Figure 4, "Y > Y acc", and associated text in Section 6)

modifying said simulating according to said correlation data.
(Strojwas, especially: Figure 3, "Tuner (Nonlinear Stochastic Optimizer)", and associated text in Sections 4 and 5; Figure 4, "Optimize Design Rules", and associated text in Section 6)

20. In regards to Claim 9, Strojwas teaches the following limitations:

9. A method of correcting a hardware modeling process, said method comprising:

manufacturing devices based on design criteria;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that one must manufacture devices in order to obtain "data fabrication lines" and to "defect statistics".

measuring features of said devices to produce measured features;

(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that one must measure features in order to obtain data and statistics.

isolating a portion of said modeling process;
(Strojwas, especially: Figure 3, "Observed Distributions", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that only the measured aspects of modeling process are used in tuning / optimization of the model. Examiner finds this corresponds to "isolating a portion of the modeling process."

supplying at least one of said measured features to said portion of said modeling process,
(Strojwas, especially: Figure 3, "Observed Distributions", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

wherein said portion of said modeling process outputs a simulated result;
(Strojwas, especially: Figure 3, "Performance Distributions", and associated text in Sections 4 and 5; Figure 4, "Design Rules", and associated text in Section 6)

comparing said simulated result to a corresponding measured feature of said measured features; and
(Strojwas, especially: Figure 3, "Do They Match?" and associated text in Sections 4 and 5; Figure 4, "Y > Y acc", and associated text in Section 6)

calculating a correction to said portion of said modeling process based on said comparing.
(Strojwas, especially: Figure 3, "Tuner (Nonlinear Stochastic Optimizer)", and associated text in Sections 4 and 5; Figure 4, "Optimize Design Rules", and associated text in Section 6)

21. In regards to Claim 12, Strojwas expressly teaches the following limitations:

12. The method in claim 9, further comprising repeating said method for second portions of said modeling process to produce second corrections.
(Strojwas, especially: Figure 3, "Do They Match?", "Tuning Complete" and associated text in Sections 4 and 5; Figure 4, "Y > Y acc", and associated text in Section 6)

22. In regards to Claim 13, Strojwas expressly teaches the following limitations:

13. The method in claim 12, further comprising modifying said modeling process based on said correction and said second corrections, such that said modeling process automatically makes said corrections after performing a simulation.

(Strojwas, especially: Figure 3, "Do They Match?", "Tuning Complete" and associated text in Sections 4 and 5; Figure 4, "Y > Y acc", and associated text in Section 6)

23. In regards to Claim 30, Strojwas teaches the following limitations:

30. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for performing model to hardware correlation, comprising:

simulating models based upon design criteria;
(Strojwas, especially: Figure 3, "Performance Distributions", and associated text in Sections 4 and 5; Figure 4, "Design Rules", and associated text in Section 6)

manufacturing devices based upon said design criteria;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that one must manufacture devices in order to obtain "data fabrication lines" and to "defect statistics".

evaluating features of said devices during said manufacturing to produce in-line test parametric data;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that one must measure ("evaluate") features in order to obtain data and statistics.

comparing said models to said in-line test parametric data to obtain correlation data; and
(Strojwas, especially: Figure 3, "Do They Match?" and associated text in Sections 4 and 5; Figure 4, "Y > Y acc", and associated text in Section 6)

modifying said simulating according to said correlation data.
(Strojwas, especially: Figure 3, "Tuner (Nonlinear Stochastic Optimizer)", and associated text in Sections 4 and 5; Figure 4, "Optimize Design Rules", and associated text in Section 6)

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. The prior art used for these rejections is as follows:

26. Strojwas, A.J., "Design for Manufacturability and Yield". Proc. of the 26th ACM/IEEE Conf. on Design Automation. 1989. pp.454-459. (Henceforth referred to as "**Strojwas**").

27. Michael, C. et al. "A Flexible Statistical Model for CAD of Submicrometer Analog CMOS Integrated Circuits." Proc. of the 1993 IEEE/ACM Int'l Conf. on CAD. 1993. pp.330-333. (Henceforth referred to as "**Michael**").

28. Bryant et al., U.S. Patent 6,239,591. (Henceforth referred to as "**Bryant**").

29. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

30. Claims 3-5, 10, 14-17 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strojwas in view of Michael.

31. In regards to Claim 3, Strojwas does not expressly teach the following limitations:

> 3. The method in claim 1, wherein said modifying produces a modified simulation and said method further comprises identifying, in a characterization map, ones of said devices that match models produced by said modified simulation.

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches that "These figures indicate that the new statistical model and its implementation in HSPICE can reproduce in a circuit simulation the statistical

device characterization data inputted to the model." (See Section 4, "Simulation", and also Figures 4 and 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

32. In regards to Claim 4, Strojwas teaches the following limitations:

4. The method in claim 1, wherein:
said devices comprise semiconductor devices;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

However, Strojwas does not expressly teach the following limitations:

said models include modeled threshold voltage values;
said in-line test parametric data includes test threshold voltage values;
said comparing compares said modeled threshold voltage values and said test threshold voltage values to produce a threshold voltage adder; and
said modifying includes adding said threshold voltage adder to said modeled threshold voltage values.

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches that "... a simple four parameter drain current model for an n-channel transistor operating in the saturating region is used to describe statistical device variations ..." (See Section 2, Eq. 1). One of the parameters is "the zero

V_{BS} threshold voltage, V_{TO} ...". (See Section 2). Moreover, "Figure 2 shows an example of the fit of $\sigma(\Delta V_{T0})$ to Eq. (6)." (See p.332, Section 3.1)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

33. In regards to Claim 5, Strojwas teaches the following limitations:

5. The method in claim 1, wherein:
said devices comprise semiconductor devices;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

However, Strojwas does not expressly teach the following limitations:

said models include modeled saturated current values;
said in-line test parametric data includes test saturated current values;
said comparing compares said modeled saturated current values and said test saturation saturated current values to produce a saturated current error value.

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches that "... a simple four parameter drain current model for an n-channel transistor operating in the saturation region is used to describe statistical

variations ..." (See Section 2, Eq. 1). The dependent variable in this equation, Eq. 1 is "I_D", the drain current.

Moreover, Michaels also teaches an additional equation for modeling an "I_D" (See Section 3, Eq.4) and "... By using this method, the statistical model is separated from the nominal SPICE model." (See Section 3). Michaels teaches that "Figure 4 shows a comparison between simulated and measured drain current mismatch standard deviation for one NMOS transistor per pair." (See section 4, col.2, paragraph 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

34. In regards to Claim 10, Strojwas does not expressly teach the following limitations:

10. The method in claim 9, wherein said simulated result and said corresponding measured feature comprise one of a voltage, current, and physical dimension.

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches that "... a simple four parameter drain current model for an n-

channel transistor operating in the saturation region is used to describe statistical variations ..." (See Section 2, Eq. 1). The dependent variable in this equation, Eq. 1 is "I_D", the drain current. Two of the dependent parameters are V_{BS}, a voltage parameter, and Λ, channel length modulation, a physical dimension.

Moreover, Michaels also teaches an additional equation for modeling an "I_D" (See Section 3, Eq.4) and "... By using this method, the statistical model is separated from the nominal SPICE model." (See Section 3). Michaels teaches that "Figure 4 shows a comparison between simulated and measured drain current mismatch standard deviation for one NMOS transistor per pair." (See section 4, col.2, paragraph 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

35. In regards to Claim 14, Strojwas does not expressly teach the following limitations:

> 14. The method in claim 9, wherein said measuring comprises measuring physical dimensions and performance operations of said devices at different points of said manufacturing of said devices.

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches that "... a simple four parameter drain current model for an n-channel transistor operating in the saturation region is used to describe statistical variations ..." (See Section 2, Eq. 1). The dependent variable in this equation, Eq. 1 is "I_D", the drain current. Two of the dependent parameters are V_{BS}, a voltage parameter, and Λ, channel length modulation, a physical dimension.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

36. In regards to Claim 15, Strojwas does not expressly teach the following limitations:

15. The method in claim 9, further comprising performing a statistical analysis based on results of said comparing process.

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches an addition equation for modeling an "I_D" (See Section 3, Eq.4) and "... By using this method, the statistical model is separated from the nominal SPICE model." (See Section 3). Michaels teaches that "Figure 4 shows a

comparison between simulated and measured drain current mismatch standard deviation for one NMOS transistor per pair." (See section 4, col.2, paragraph 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

37. In regards to Claim 16, Strojwas teaches the following limitations:

16. A method of performing model to hardware correlation for semiconductor chips, comprising:
obtaining fabrication in-line parametric data;
extracting first parameters from said parametric data to make a first set of go-data;

(Strojwas, especially: Figure 3, "Do They Match?" and associated text in Sections 4 and 5; Figure 4, "Y > Y acc", and associated text in Section 6)

Strojwas teaches in Fig.3 that the use of the "Tuner" can be repeated several times.

Moreover, Strojwas also teaches the following limitations:

calculating **a threshold voltage adder** from said first comparing; and
correcting said modeling program using said **threshold voltage adder**.

Strojwas teaches (see Section 5, p.457) the use of "Adjustment factors" which "... can be used to move the expected value (mean) of performance to

desired target values). Examiner interprets that the adjustment factor corresponds to Applicant's "threshold voltage adder".

However, Strojwas does not expressly teach the following limitations:

calculating a first simulated threshold voltage saturation and first simulated saturated source/drain current based on said first set of go-data using a modeling program;

performing a first comparing of said first simulated threshold voltage saturation to an in-line parametric threshold voltage saturation from said parametric data and a first comparing of said first simulated saturated source/drain current to an in-line parametric saturated source/drain current from said parametric data;

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches that "... a simple four parameter drain current model for an n-channel transistor operating in the saturation region is used to describe statistical variations ..." (See Section 2, Eq. 1). The dependent variable in this equation, Eq. 1 is "I_D", the drain current. Two of the dependent parameters are V_{BS}, a voltage parameter, and Λ, channel length modulation, a physical dimension.

Moreover, Michaels also teaches an additional equation for modeling an "I_D" (See Section 3, Eq.4) and "... By using this method, the statistical model is separated from the nominal SPICE model." (See Section 3). Michaels teaches that "Figure 4 shows a comparison between simulated and measured drain current mismatch standard deviation for one NMOS transistor per pair." (See section 4, col.2, paragraph 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer

processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

38. In regards to Claim 17, However, Strojwas does not expressly teaches the following limitations:

17. The method in claim 16, further comprising

adding said threshold voltage adder to said first set of go-data to make a second set of go-data;

calculating a second simulated threshold voltage saturation and second simulated saturated source/drain current based on said second set of go-data using said modeling program;

performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current;

verifying that said threshold voltage adder corrected said second simulated threshold voltage saturation and said second simulated saturated source/drain current.

Michaels, on the other hand, does expressly teach these limitations. Michaels teaches that "... a simple four parameter drain current model for an n-channel transistor operating in the saturating region is used to describe statistical device variations ..." (See Section 2, Eq. 1). One of the parameters is "the zero V_{BS} threshold voltage, V_{TO} ...". (See Section 2). Moreover, "Figure 2 shows an example of the fit of $\sigma(\Delta V_{T0})$ to Eq. (6)." (See p.332, Section 3.1)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer

processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

39. **Claims 32-34 are rejected based on the same reasoning as claims 3-5, *supra*. Claims 32-34 are program storage device claims reciting the equivalent limitations as are recited in method claims 3-5 and taught throughout Strojwas and Michael.**

40. **Claims 2, 6, 7, 11, 31 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Strojwas in view of Michael and further in view of Bryant.**

41. In regards to Claim 2, Strojwas does not expressly teach the following limitations:

> 2. The method in claim 1, wherein said simulating produces geometric, DC, AC, and delay stage simulated parameters, and wherein said in-line test parametric data includes geometric, DC, AC, and delay stage test parameters.

The Michael reference expressly teaches that the in-line test parametric data includes geometric test parameters such as gate length and channel length (p.331, col.2, Section 3.1, paragraphs 2-3), and also DC test parameters such as standard drain current (p.331, col.2, Section 3, paragraph 2), and threshold voltage (p.330, col.2, Section 2, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer

processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

Moreover, the Bryant reference teaches the use of delay stage test parameters (Bryant, col.2, lines 49-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Bryant, because "It is commonly known that the SOI floating body results in hysterises effects whereby the delay through a set of SOI circuits depends on the input history. Manufacturing control of this history effect is crucial."

42. In regards to Claim 6, Strojwas teaches the following limitations:

6. The method in claim 1, wherein:
said devices comprise semiconductor devices;
(Strojwas, especially: Figure 3, "Data from Fabrication Line", and associated text in Sections 4 and 5; Figure 4, "Defect Statistics", and associated text in Section 6)

It is inherent that one must manufacture devices in order to obtain "data fabrication lines" and to "defect statistics".

However, Strojwas does not expressly teach the following limitations:

said models include modeled delay per stage values;
said in-line test parametric data includes test delay per stage values;
said comparing compares said modeled delay per stage values and said test saturation delay per stage values to produce a delay per stage error value.

43. In regards to Claim 7, Strojwas does not expressly teach the following limitations:

7. The method in claim 1, further comprising culling said in-line test parametric data to retain selected geometric, D.C., A.C. and delay test parameters.

The Michael reference expressly teaches that the in-line test parametric data includes geometric test parameters such as gate length and channel length (p.331, col.2, Section 3.1, paragraphs 2-3), and also DC test parameters such as standard drain current (p.331, col.2, Section 3, paragraph 2), and threshold voltage (p.330, col.2, Section 2, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

Moreover, the Bryant reference teaches the use of delay stage test parameters (Bryant, col.2, lines 49-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Bryant, because "It is commonly known that the SOI floating body results in hysterises effects whereby the delay through a set of SOI circuits depends on the input history. Manufacturing control of this history effect is crucial."

44. In regards to Claim 11, Strojwas does not expressly teach the following limitations:

> 11. The method in claim 9, wherein said portion of said modeling process simulates an integrated circuit design to model one of saturation threshold voltage, saturated source/drain current, and delay per stage.

The Michael reference expressly teaches that the in-line test parametric data includes geometric test parameters such as gate length and channel length (p.331, col.2, Section 3.1, paragraphs 2-3), and also DC test parameters such as standard drain current (p.331, col.2, Section 3, paragraph 2), and threshold voltage (p.330, col.2, Section 2, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Michaels, because "Unfortunately, due to greater relative variations in fabrication steps such as gate oxide growth and photolithography, devices in these submicrometer processes have greater parametric variation compared to those in older technologies" (Michaels, p.330, col.1, paragraph. 1) and "This paper presents a flexible and accurate statistical model for submicrometer analog circuit applications which can easily be implemented in existing circuit simulation tools" (Michaels, p.330, col.1, paragraph. 1).

Moreover, the Bryant reference teaches the use of delay stage test parameters (Bryant, col.2, lines 49-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Strojwas with those of Bryant, because "It is commonly known that the SOI floating body results in hysterises

effects whereby the delay through a set of SOI circuits depends on the input history. Manufacturing control of this history effect is crucial."

45. **Claims 31 and 35-36 are rejected based on the same reasoning as claims 2 and 6-7, *supra*. Claims 31 and 35-36 are program storage device claims reciting the equivalent limitations as are recited in method claims 2 and 6-7 and taught throughout Strojwas, Michael and Bryant.**

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone numbers are (703) 306-0297 *[Before Oct. 25, 2004]* and (571) 272-3714 *[After Oct. 25, 2004].* The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (703) 305-9704 *[Before Oct. 25, 2004]* and (571) 272-3716 *[After Oct. 25, 2004].*

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose

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October 13, 2004

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